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(54) Abstract Title
Thin film transistor

(57) The thin film transistor has a gate electrode 12 which extends over a lightly doped drain (LDD) region 5. The intensity of the electric field across the intrinsic channel - LDD junction and the LDD - drain region junction is controlled by grading the dopant concentration in the channel/drain region (figure 4). A graduated change in impurity concentration between the intrinsic channel region and the LDD region may be obtained by dopant implantation using a mask having a tapered thickness profile (figure 2). This gate overlapped LDD structure reduces instabilities caused by high drain fields whilst avoiding an increase in series resistance and a decrease in TFT transconductance.

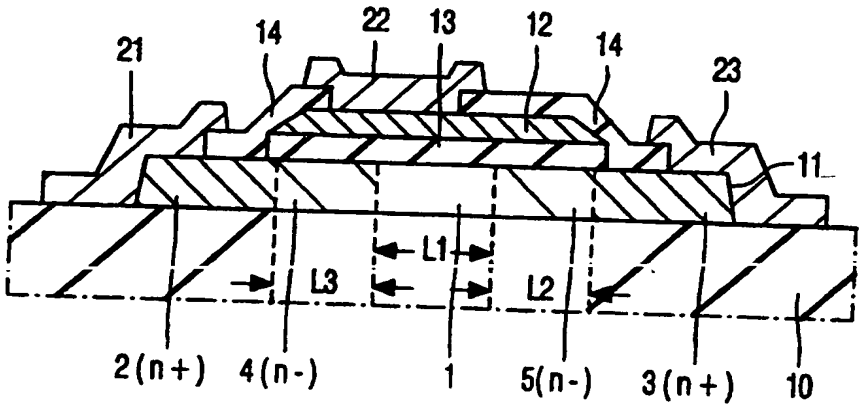

FIG. 1

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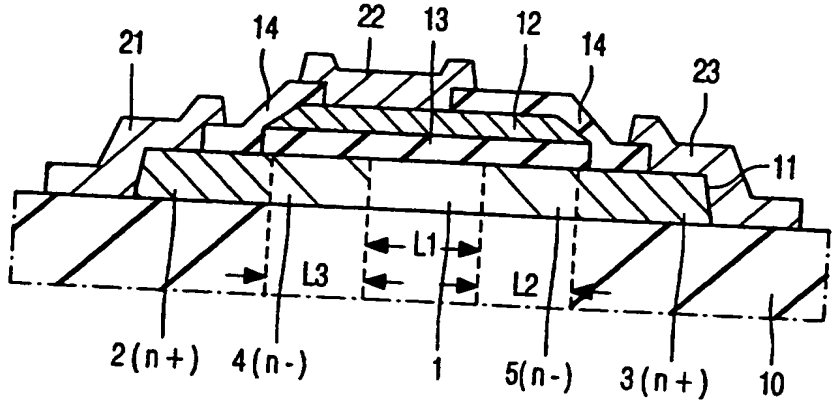

FIG. 1

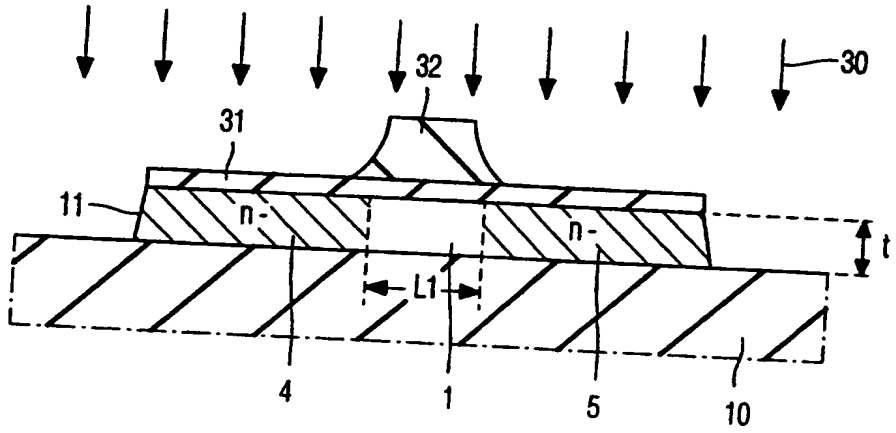

FIG. 2

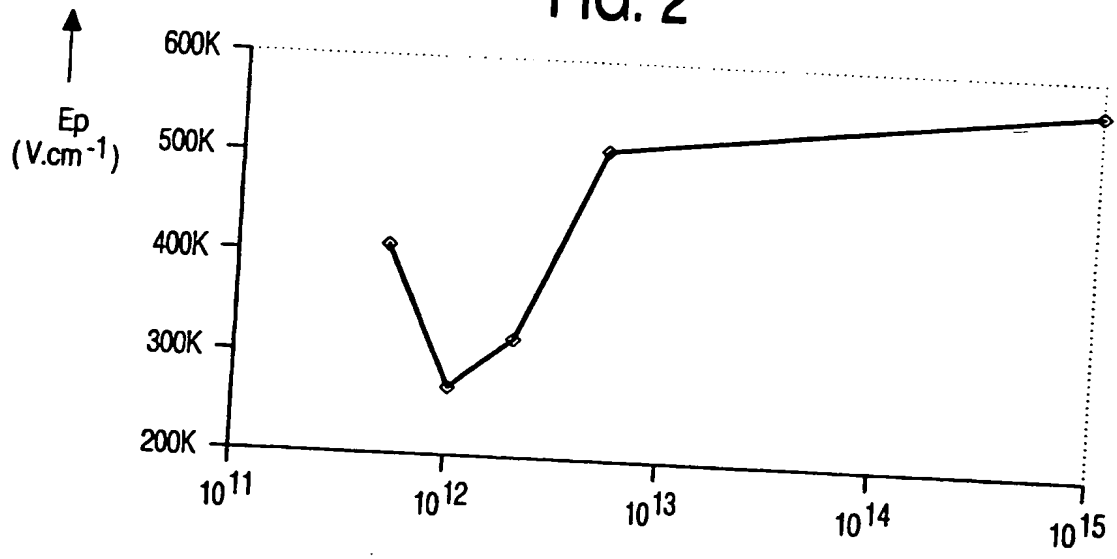

FIG. 3

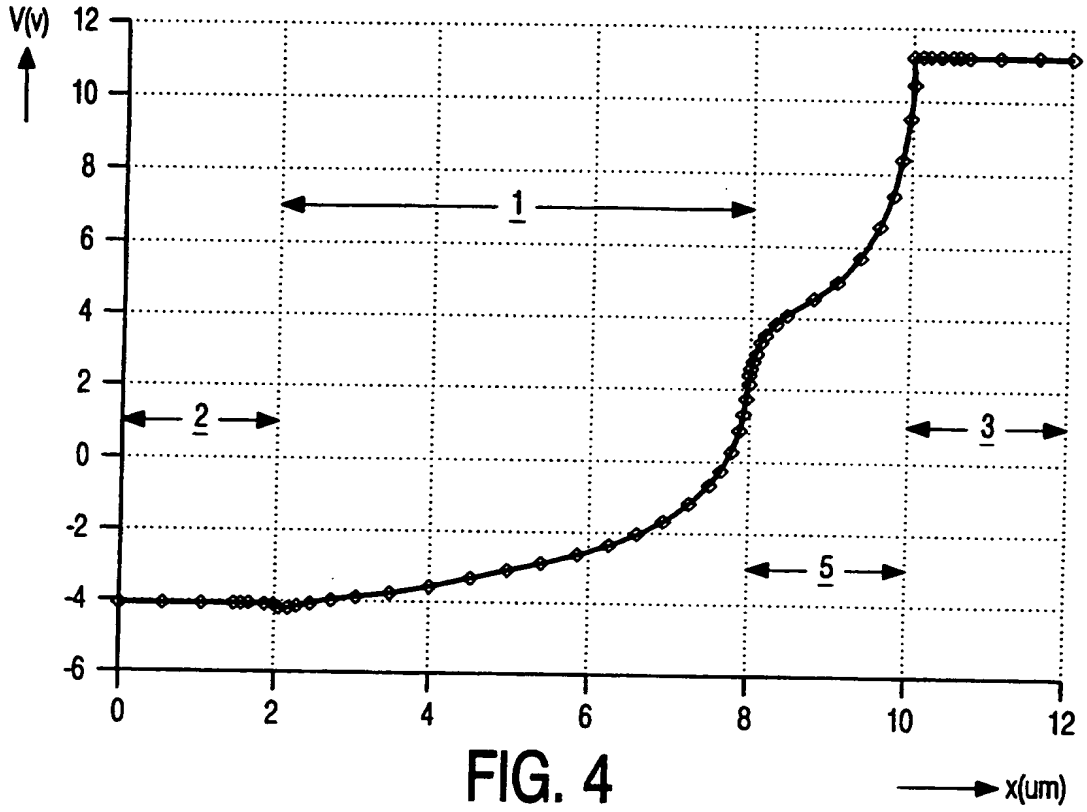
V(v)
12
10
8
6
4
2
0
-2
-4
-6
0
2
4
6
8
10
12
1
2
3
5
x(um)

FIG. 4

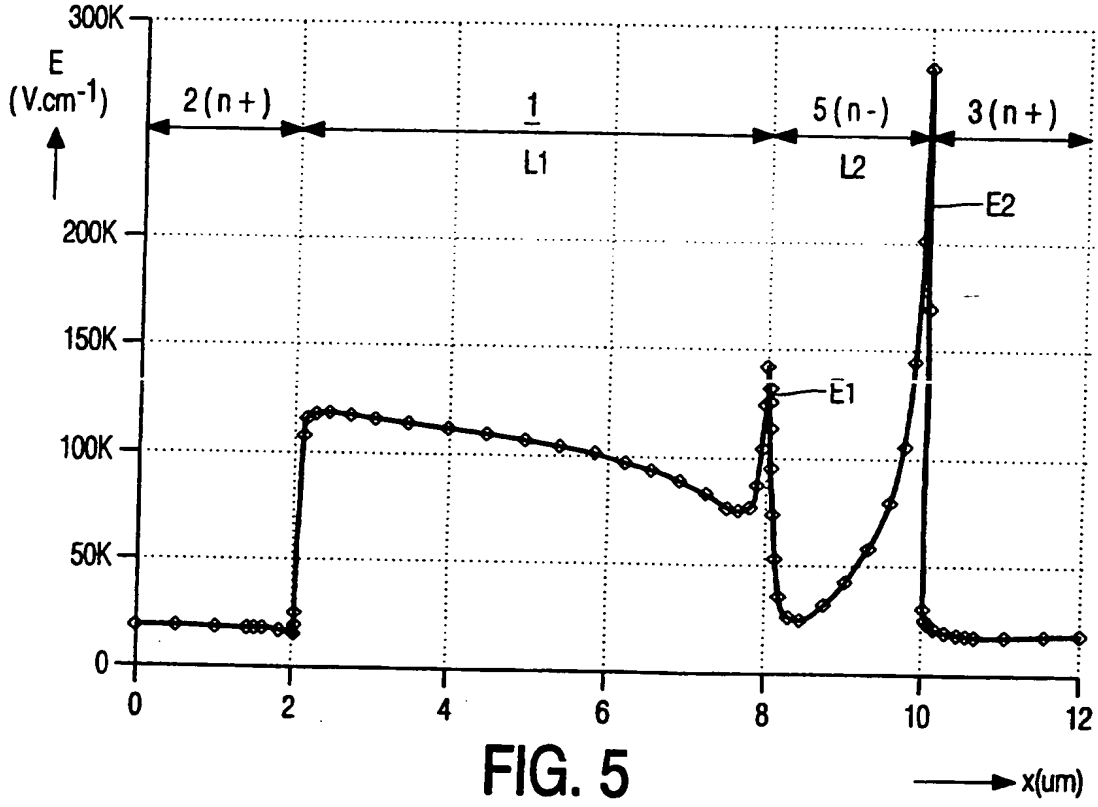
300K
E
(V.cm-1)
200K
150K
100K
50K
0
2(n+)
1
L1
5(n-)
L2
3(n+)
E2
E1
0
2
4
6
8
10
12
x(um)

FIG. 5

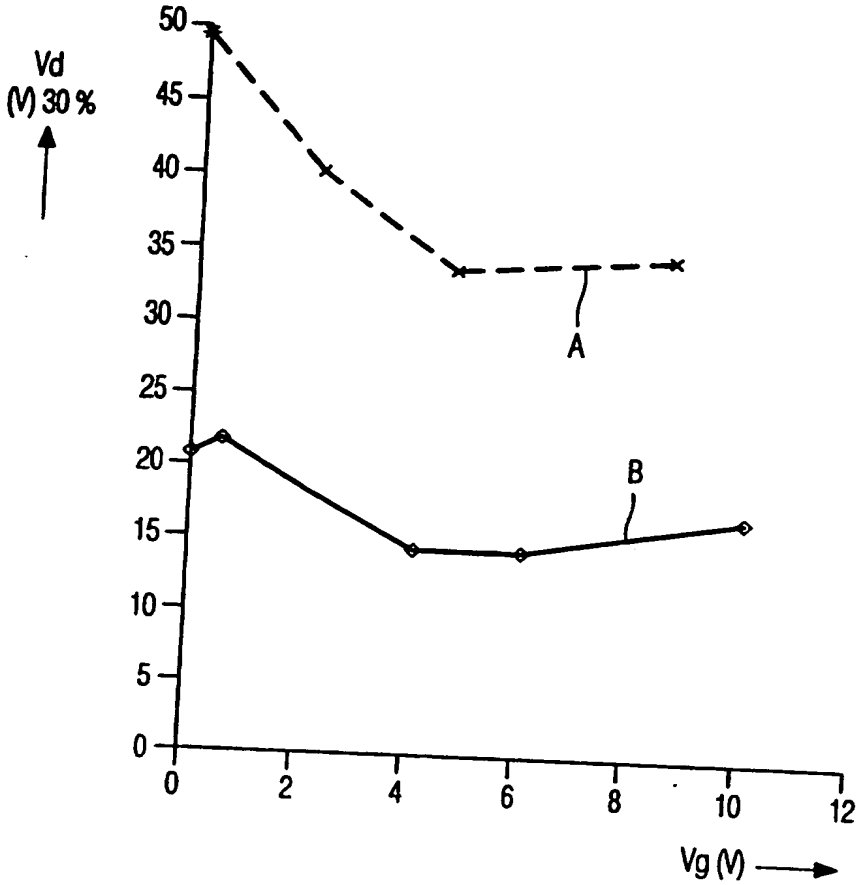

FIG. 6

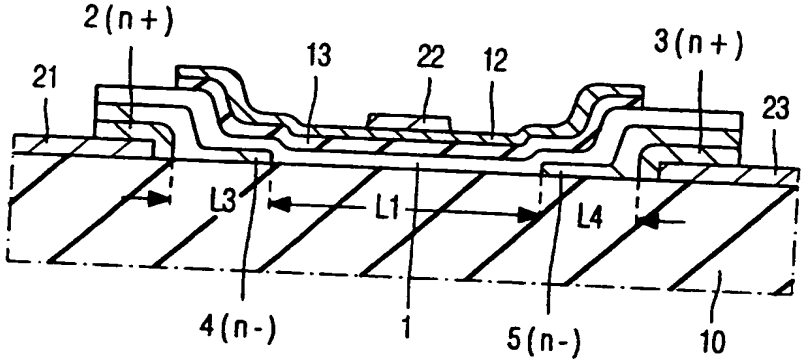

FIG. 7

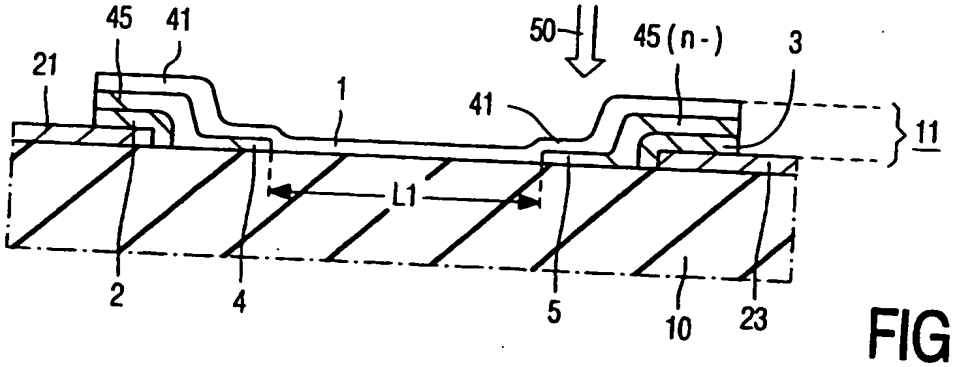

FIG. 8

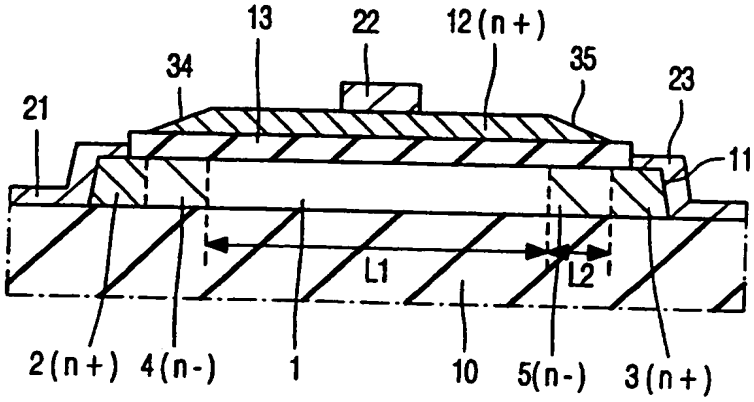

FIG. 9

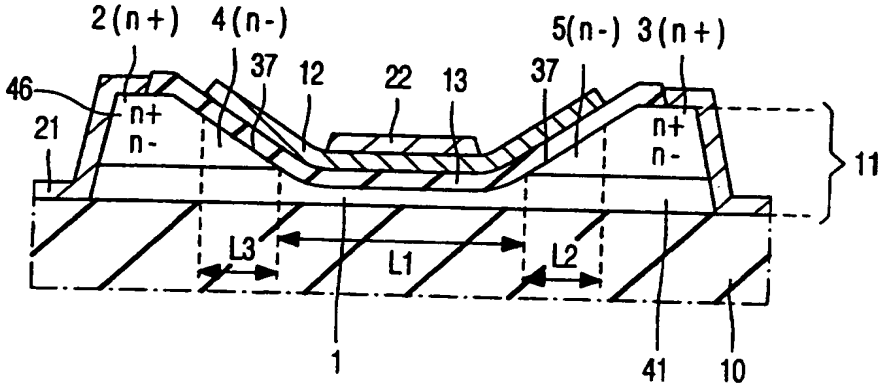

FIG. 10

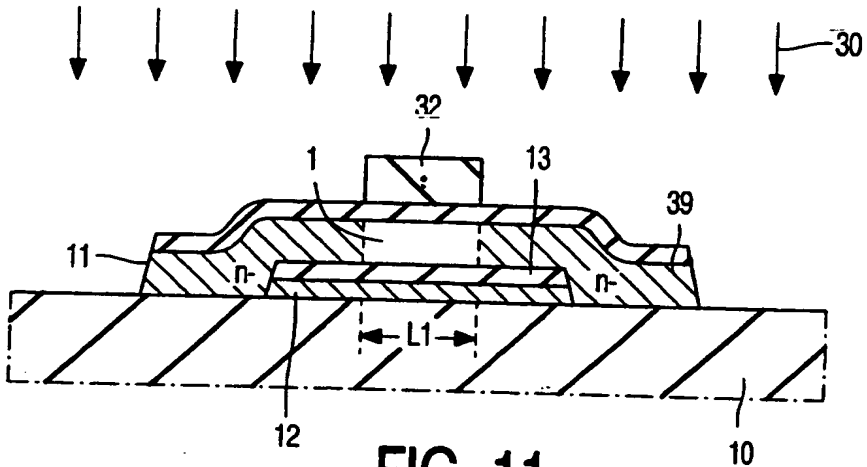

FIG. 11

DESCRIPTION

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ELECTRONIC DEVICES COMPRISING THIN-FILM TRANSISTORS, AND THEIR MANUFACTURE.

This invention relates to electronic devices including thin-film circuit elements which comprise a semiconductor film pattern on an insulating substrate, one of the circuit elements being a thin-film field-effect transistor (hereinafter termed "TFT"). The device may be, for example, an active-matrix liquid-crystal display or other flat panel display, or any other type of large area electronic device with TFTs, for example, a thin-film data store or an image sensor. The invention also relates to methods of manufacturing such an electronic device.

There is currently much interest in developing thin-film circuits with TFTs on glass and on other inexpensive insulating substrates, for large area electronics applications. Such TFTs fabricated with amorphous or polycrystalline semiconductor films may form the switching elements of a cell matrix, for example, in a flat panel display as described in United States Patent US-A-5 130 829 (Our Ref: PHB 33646), the whole contents of which are hereby incorporated herein as reference material. A recent development involves the fabrication and integration of circuits from TFTs (often using polycrystalline silicon) as, for example, integrated drive circuits for such a cell matrix. Unfortunately, field-induced instabilities occur in the transistor characteristics of such TFTs, especially those fabricated with polycrystalline silicon formed using low temperature processes. Several instability mechanisms occur, for example, bias-induced state creation in the polycrystalline silicon, hot carrier induced state creation and carrier trapping, and drain field-enhanced leakage current. The degradation of the transistor characteristics (for example, off-state leakage current, threshold voltage and on-state current) can seriously limit the use of such TFTs in such circuits.

Published European Patent Application EP-A-0 520 560 (Our Ref: PHB 33726) discloses one way of reducing such instabilities of TFTs in an electronic

device. The thin-film field-effect transistor has a gate electrode which overlaps and is coupled to an undoped channel region of a semiconductor film pattern on an insulating substrate for controlling current flow through the channel region. The transistor has a field-relief region of one conductivity type between the undoped channel region and a drain region of the one conductivity type, the conductivity type determining doping concentration of the field-relief region being lower than that of the drain region. This field-relief region is not overlapped by the drain region nor modulated by the gate electrode, and it extends from the drain region longitudinally towards the gate electrode in an area of lateral separation between the gate electrode and the drain region.

Although such a field-relief region is effective in reducing the instability effects, the transconductance of the TFT is reduced due to the increased series resistance arising from the unmodulated length of the field-relief region in this area of lateral separation. The increase in series resistance can be quite significant due to the high density of trapping states in the polycrystalline or amorphous silicon film (or films) in which the undoped channel region and the low-doped field-relief region are provided. Measurement of these trapping states and their distribution and their effect is described in the article "Characterisation Of Trapping States In Polycrystalline-Silicon Thin-Film Transistors By Deep Level Transient Spectroscopy" by the present inventor, published in Journal of Applied Physics 74(3), 1 August 1993, pages 1787 to 1792, the whole contents of which are hereby incorporated herein as reference material.

It is an aim of the present invention to provide a different arrangement of a field-relief region at the drain of a TFT, which reduces instabilities due to high drain field while avoiding or reducing an increase in series resistance and a decrease in TFT transconductance, even with a high density of trapping states.

According to one aspect of the present invention there is provided an electronic device including thin-film circuit elements which comprise a semiconductor film pattern on an insulating substrate, one of the circuit

elements being a thin-film field-effect transistor having a gate electrode which overlaps and is coupled to an undoped channel region of the semiconductor film pattern for controlling current flow through the channel region, wherein the transistor has a field-relief region of one conductivity type between the undoped channel region and a drain region of the one conductivity type, the conductivity type determining doping concentration of the field-relief region being lower than that of the drain region, wherein the gate electrode overlaps and is coupled to the field-relief region (preferably over substantially the entire length of the field-relief region between the channel region and the drain region), the overlapped length of the field-relief region being larger than the thickness of the semiconductor film pattern.

In such a transistor structure in accordance with the present invention the gate electrode overlaps and is coupled to the field-relief region, and so the conductance of the field-relief region is modulated by the gate electrode in the on-state of the transistor. Hence, an increase in series resistance due to the inclusion of this overlapped-field relief region is mitigated. However, the potential drop between the undoped channel region and the highly doped drain region is distributed along the length of field-relief region overlapped by the gate, so reducing the high electric field in this area and thereby reducing instabilities resulting from such a high field in both the on-state and off-state of the transistor. In order to obtain the desired degree of field relief, the overlapped length of the field-region may typically be an order of magnitude larger than the thickness of the semiconductor film pattern, given the very high density of charge-carrier trapping states in the semiconductor film pattern of such TFTs, and given typical values for the thickness of the semiconductor film pattern and for the degree of coupling by the gate electrode of the TFT. Thus, the overlapped length of the field-relief region is typically of the order of a micrometre (micron), for example from about 1μm to several micrometres.

In a device in accordance with the present invention, the high electric field between the gate electrode, the undoped channel region and the highly doped drain region is reduced by distributing the potential drop along the significant length (about 1μm to several micrometres) of the field-relief region

overlapped by the gate. Typically, the electric field along this large overlapped length of field-relief region exhibits a first peak between the channel region and field-relief region and a second peak between the field-relief region and the drain region. By adjusting the doping concentration of the field-relief region, it is possible to control which of the first and second peaks is of a higher intensity. Thus, for example, when the field-relief region is of a uniform doping concentration with a uniform density of trapping states, the intensity of the second peak can be reduced relative to the first peak by increasing the doping concentration of the field-relief region, and vice versa. The intensity of each peak can also be reduced by grading the doping concentration in the vicinity of that peak. Thus, the doping concentration between the field-relief region and the drain region may be graded to reduce the intensity of the second peak. The doping concentration of the field-relief region may be graded into the channel region to reduce the intensity of the first peak.

According to the second aspect of the present invention there are provided various methods of manufacturing such an electronic device. The gate electrode may be formed overlapping the field-relief region by providing a conductive film portion on a dielectric film over the field-relief region after forming the field-relief region with its said lower doping concentration. However the TFT may be of an inverted configuration, in which the gate electrode is formed on the insulating substrate before depositing and forming the semiconductor film pattern, and the field-relief region with its said lower doping concentration may be formed subsequently to overlap the gate electrode.

Various process technologies may be used to grade the doping concentration of the field-relief region. The doping concentration may be graded progressively along the length of the field-relief region. Alternatively, most of the length of the field-relief region may be of substantially uniform doping concentration, and the graded doping concentration may be present at the interface of the field-relief region with the undoped channel region and/or the highly doped drain region.

In one form the doping concentration of the drain region may be provided by dopant ion implantation while using the gate electrode as a mask,

the edge of the gate electrode being bevelled so as to grade the implanted doping concentration from the drain region to the field-relief region. Such a process technology is particularly advantageous in providing a self-registered TFT structure in which the graded edge of the highly doped drain region is self aligned with the edge of the gate electrode.

In another form the drain region and at least the adjacent part of the field-relief region may be formed by a) depositing a semiconductor film with a doping concentration which increases progressively from the field-relief region to the drain region, and b) defining an interface between the drain region and the adjacent part of the field-relief region by etching away an area of the increased doping concentration to leave a bevelled surface between the drain region and the field-relief region. This etching step may also free the undoped channel region of an overlying deposit of the doped semiconductor film, and the overlapping gate electrode may then be provided on a dielectric film over the channel region and over the bevelled surface of the field-relief region.

In yet another form the doping concentration of the highly doped region is diffused into the field-relief region to grade the doping concentration between the field-relief region and the drain region.

These and other features of the present invention, and their advantages are illustrated specifically in embodiments of the invention now to be described, by way of example, with reference to the accompanying diagrammatic drawings, in which;

Figure 1 is a cross sectional view of a TFT structure in an electronic device in accordance with the present invention;

Figure 2 is a cross sectional view of the TFT structure of Figure 1 at a stage in its manufacture by a method in accordance with the present invention;

Figure 3 is a graph of the simulated peak drain field Ep in $V.cm^{-1}$ as a function of implantation dose d in dopant ions per cm^2 for the field-relief region of such a TFT as illustrated in Figure 1;

Figure 4 is a graph of the simulated potential V in volts with distance X in μm along the source to drain current path through such a TFT;

Figure 5 is a graph of the simulated electric field E in volts cm^{-1} with distance X in μm along the source to drain current path of such a TFT;

Figure 6 is a graph of experimental results showing the variation of a defined "degradation" value of drain voltage Vd in volts with gate voltage Vg in volts for such a TFT structure in accordance with the present invention;

Figure 7 is a cross sectional view of another TFT structure in accordance with the present invention, in which a plurality of semiconductor films are used to form the semiconductor film pattern comprising the undoped channel region, the low doped field-relief region, and the highly doped drain region of the TFT;

Figure 8 is a cross sectional view of the structure of Figure 7 at a stage in its manufacture by a method in accordance with the present invention;

Figure 9 is a cross sectional view of a further TFT structure in accordance with the present invention, in which a bevelled gate edge is used to grade the doping concentration between the highly doped drain region and lower doped field-relief region of this TFT;

Figure 10 is a cross sectional view of yet another TFT structure in accordance with the present invention, in which a bevelled surface is etched in the semiconductor film pattern between the highly doped drain region and the field-relief region of the TFT, and

Figure 11 is a cross sectional view of an inverted TFT structure in accordance with the present invention at a stage in its manufacture by a method also in accordance with the present invention.

It should be noted that, except for the graphs of Figures 3 to 6, all the drawings are diagrammatic and not drawn to scale. Relative dimensions and proportions of parts of these Figures 1, 2, and 7 to 11 have been shown exaggerated or reduced in size for the sake of clarity and convenience in the drawings. The same reference signs are generally used to refer to corresponding or similar features in the different embodiments.

The TFT of Figure 1 comprises an island of a semiconductor film pattern 11 on an insulating substrate 10. The TFT has a gate electrode 12 which overlaps and is coupled to an undoped channel region 1 of the semiconductor

film pattern 11. Thus the gate electrode 12 serves in known manner for controlling current flow through the channel region 1 between source and drain regions 2 and 3 of the TFT. The transistor of Figure 1 has a field-relief region 5 of one conductivity type (n-type in the example shown) between the undoped channel region 1 and the highly doped drain region 3 also of the one conductivity type. The conductivity type determining doping concentration (n-) of the field-relief region 5 is lower than that (n+) of the drain region 3. In the particular example of Figure 1 a symmetrical TFT configuration is shown, in which a similarly lowly-doped region 4 is present between the highly doped source region 2 and the undoped channel region 1.

In accordance with the present invention the gate electrode 12 overlaps and is coupled to the field-relief region 5 over substantially the entire length L2 of the field relief region 5 between the channel region 1 and the drain region 3. This overlapped length L2 of the field relief region 5 is an order of magnitude larger than the thickness t of the semiconductor film pattern 11. By this means, the conductance through the field-relief region 5 is modulated by the gate electrode 12 in the on-state of the TFT, while the potential drop (and hence the high electric field) between the undoped channel region 1 and the highly doped drain region 3 in both the off-state and the on-state of the TFT is distributed along the large length L2 of the field-relief region 5 overlapped by the gate 12. Where a low-doped region 4 is also provided between the source region 2 and the channel region 1, the gate electrode 12 is arranged to overlap this region 4 as well as the region 5 so that both the regions 4 and 5 (as well as the channel region 1) are modulated by the gate voltage.

This TFT forms part of a large-area electronic device, for example, a flat panel display as illustrated in US-A-5130 829, or a large-area image sensor, or a data store. This large-area device includes a large number of circuit elements formed in and on the semiconductor film pattern 11 on the insulating substrate 10. The thin-film circuitry may comprise, for example, TFT drive circuits and a matrix of TFT switching transistors. In the case of a flat panel display as described in US-A-5 130 829, the substrate 10 may be a back plate of the display. The device substrate 10 is electrically insulating at least

adjacent to its top surface. The substrate 10 may comprise a glass or other low-cost insulating material. In a particular embodiment, it may comprise an upper layer of silicon dioxide on a glass base. In most typical cases, the substrate 10 is only capable of withstanding temperatures of less than 700°C (celsius), for example up to 625°C for a glass of moderate quality and cost, or as low as about 200°C for a poorer quality glass or for a plastics material. A large number of the individual TFTs of Figure 1 are generally formed side by side on the device substrate 10 and are interconnected by thin-film conductor patterns such as metal tracks, 21, 22, 23. These tracks 21,22,23 etc extend from the individual TFT islands onto and across the substrate 10.

The film pattern 11 may be of polycrystalline silicon having a thickness t in the range of about 40 nm (nanometers) to 0.1 μm (micrometres). This film pattern 11 may be formed in known manner by depositing a silicon film on the substrate 10 and subsequently etching the film to form the desired island pattern for the TFTs. The silicon film may be deposited by a low pressure chemical vapour deposition (LPCVD) process or a plasma-enhanced chemical vapour deposition (PECVD) process. At a deposition temperature of about 620°C or less with LPCVD or 350°C or less with PECVD, a polycrystalline silicon film is formed in situ on the substrate. With a lower temperature e.g. less than 550°C with a LPCVD process, or between 200°C and 300°C with a PECVD process) amorphous silicon material is deposited. This amorphous silicon material may be crystallised into polycrystalline material in known manner, by heating the structure in a furnace to about 600°C or by heating the film with a laser beam. It is also possible to use a very low cost process (such as evaporation or sputter deposition) to deposit the silicon material which is then crystallised to better quality material in such a heating step.

The polycrystalline silicon material resulting from all these processes has a high density of charge-carrier trapping states, even when the material comprises large crystal grains such as can be formed by furnace annealing. The deposited material contains no deliberate doping, but its conductivity is determined by the high density of trapping states. These trapping states result in the Fermi level being pinned near the middle of the energy band gap, so that

the conductivity of the polycrystalline material is effectively intrinsic or very slightly n-type in some polycrystalline forms. An area of this undoped material is retained to form the channel region 1 of the TFT.

Figure 2 illustrates a stage in the manufacture of the TFT of Figure 1 in which a low doping concentration n- (for example, of phosphorous or another donor impurity) is introduced into the undoped polycrystalline silicon film material. The channel region 1 is masked against this donor doping step. In the specific example of Figure 2, this doping step is carried out by implantation of donor ions 30 through an insulating layer 31 on the surface of the silicon film island 11. The channel region 1 is masked against the implantation by a masking pattern 32. The masking pattern 32 may be of for example photoresist. The insulating layer 31 may be of the same dielectric material and thickness as required for the gate dielectric 13 of the TFT of Figure 1. Typically, the layer 13 (and 31) may be of silicon dioxide having a thickness in the range of about 0.1μm to 0.2μm. Thus, after the implantation step illustrated in Figure 2, the masking pattern 32 may be removed from the dielectric layer 31, and the gate electrode may be formed by providing a conductive film portion 12 on the dielectric film 31. This conductive film portion 12 is provided over the channel region 3 and over the implanted areas for the regions 4 and 5.

The conductive film portion 12 may be of metal, or it may be of silicon which is doped to a highly conductive state during the subsequent doping step used to form the source and drain regions 2 and 3. The film portion 12 on the dielectric layer 13 or 31 may serve as an implantation mask during the formation of the highly-doped source and drain regions 2 and 3 by dopant ion implantation in known manner. Typically the doping concentration of the source and drain regions 2 and 3 (and of a silicon gate electrode 12) is of the order of 10^{20} or 10^{21} phosphorous atoms cm^{-3}. A further dielectric film 14 (for example of silicon dioxide) is deposited over the gate electrode 12, after which contact windows for the source, drain and gate are opened in the dielectric films 14 and 13 (31). The conductor tracks 21, 22, 23 are then provided to contact the highly-doped source region 2, gate electrode 12, and drain region

3. The TFT structure of Figure 1 is thereby formed.

In the embodiment described so far with reference to Figures 1 and 2, a similar overlapped low-doped region 4 is shown between the highly source region 2 and the undoped channel region 1, in addition to the overlapped low-doped field-relief region 5 between the channel region 1 and the drain region 3. The resulting TFT is symmetrical in operation with respect to its source and drain. However, where a symmetrical TFT structure is not required, the low-doped region 4 may be omitted in favour of an extension of the undoped channel region 1 to abut the highly doped source region 2. This non-symmetrical structure can be fabricated by adopting a wider mask 32 for the channel region 1 in Figure 2, and by arranging the gate electrode 13 so that it does not overlap the low doped implant at the source end of the channel region 1 whereby the source region 2 when formed by the subsequent self-aligned implantation abuts the undoped channel region 1. A non-symmetrical TFT model of this type was used for the simulations of Figures 3 to 5, with the following dimensions chosen by way of a specific example:

Length L1 of 6μm for the undoped channel region 1;
Length L2 of 2μm for field-relief region 5;
Length L3 of zero, i.e no region 4;
Length of 8μm for gate electrode 12;
thickness t of 40 nm for silicon film 11;
thickness of 0.15μm for gate dielectric 13.

The high density of trapping states in the polycrystalline silicon film 11 was modelled into the simulations of Figures 3 to 5 in the form of a spatially homogeneous density of states distributed in an energy continuum through the silicon band gap, as described in the said J Applied Physics 74(3) article by the present inventor.

The doping concentration (n-) of the field-relief region 5 is very much lower than that (n+) of the drain region 3. In the absence of conductivity modulation due to the overlapping gate 12, the long length L2 of this field-relief region 5 would introduce a high series resistance into the main current path of the TFT. This series resistance problem is particularly acute due to the high

density of charge-trapping stages in the polycrystalline silicon material of the TFT island 11. The region 5 cannot have a sufficiently high doping concentration to compensate for this series resistance without adversely affecting its field-relief function, as is illustrated in Figure 3.

Figure 3 shows a simulation of how the peak value Ep of the electric field between the channel region 1 and the highly doped drain region 3 varies with the doping value d of the field-relief 5 overlapped by the gate electrode 12. The doping value d is the activated dose in cm^{-2} of implanted dopant in the region 5. In this simulation the region 5 has a length L2 of 2 μm which is overlapped by the gate electrode 12.

As can be seen from Figure 3, the optimum dose for low peak field Ep occurs in the region of 10^{12} cm^{-2}. This corresponds to a doping concentration of the order of 10^{17} cm^{-3}, with a film thickness of up to 0.1 μm. Figure 3 shows that the peak field Ep is approximately halved in value at this optimum dose. This permits the TFT of Figure 1 to be operated at approximately twice its drain voltage, without significantly increasing the field enhanced leakage current and other instabilities resulting from the high electric field. Thus a significant increase in maximum drive voltage is obtained for this TFT which has a long low-doped field-relief region 5 overlapped and modulated by the gate electrode 12.

Because the length L2 of the overlapped field-relief region 5 is very much larger than its thickness t, the electric field distribution in the region 5 with its high density of trapping states has both a vertical component dependent on the potential of the gate electrode 12 and a horizontal longitudinal component dependent on the potential drop between the channel region 1 and the drain region 3. In the on-state a good conduction channel is induced along the length L2 of the region 5, due to modulation by the gate electrode 12, so that the region 5 behaves effectively as part of the channel of the TFT. In both the on-state and the off-state a longitudinal distribution of the potential drop between regions 1 and 3 is obtained in the region 5 modulated by the gate electrode 12. In the off-state, the region 5 may be depleted vertically across the thickness t of the region 5 by the charge state induced by the potential on

the gate 12, more so than by the spread of a depletion layer from the drain region 3.

For the specific non-symmetrical TFT example having a region 5 with an overlapped length L2 of 2μm and an activated dopant dose of 10^{12} cm^{-2}, Figure 4 is a plot of the potential V along the semiconductor film pattern 11 from the source region 2 to the drain region 3. The regions 2, 1, 5 and 3 along this current path are indicated on this graph of Figure 4. The simulation of Figure 4 assumes sharp transitions in doping concentration from 10^{15} cm^{-2} in regions 2 and 3 to 10^{12} cm^{-2} in regions 4 and 5 to zero doping in region 1. The transitions were based on gaussians with a standard deviation of 10 nm. For the simulation of Figure 4, voltages of 7.5 volts and 15 volts (relative to the source 2) were assumed to be applied to the gate electrode 12 and to the drain region 3 respectively. The source region 2 is at -4 volts, and the drain region 3 is at +11 volts. Figure 4 shows how the potential difference of 15 volts between the source region 2 and the drain region 3 is dropped both in the undoped channel region 1 and in the low-doped drain region 5. The plot is taken at a depth of 2.5 nm in the film 11, where it is estimated that the peak field occurs below the interface of films 11 and 13 overlapped by the gate electrode 12. With a gate voltage Vg of 7.5 volts, the TFT is only just in the on-state, and this condition is considered to be the worst condition for degradation effects.

Figure 5 is a transformation of the simulation of Figure 4 to show the electric field intensity at this depth along the semiconductor film pattern 11 from the source region 2 to the drain region 3, instead of the potential of Figure 4. As can be seen from Figure 5, the redistribution of the potential (due to the inclusion of the overlapped field-relief region 5) results in the electric field E along the overlapped length L2 of the field-relief region 5 exhibiting a first peak E1 between the undoped channel region 1 and the low doped field-relief region 5 and a second peak E2 between the low doped field-relief region 5 and the highly doped drain region 3. These peaks E1 and E2 are considerably less in intensity than the single field peak which would occur between an undoped channel region 1 and a highly doped drain region 3 in the absence of the

overlapped field-relief region 5. Furthermore, the long length L2 of the overlapped field-relief region 5 ensures separation of the peaks E1 and E2. This separation of the peaks E1 and E2 reduces the field intensity.

The simulations of Figures 4 and 5 assumed a sharp transition in doping level between the regions 2, 1, 5, and 3. However, it is advantageous to grade the doping concentration between the field-relief region 5 and the drain region 3 so as to reduce the intensity of the second peak E2, and to grade the doping concentration of the field-relief region 5 into the channel region 1 so as to reduce the intensity of the first peak E1. This grading of the doping transitions may be achieved by diffusion of the doping levels, by prolonging a laser annealing treatment which is used to remove implantation damage in the silicon material and activate the implanted dopants. Thus, for example, after the implantation step illustrated in Figure 2, the mask 32 is removed and a laser beam is swept along the silicon film pattern 11 to anneal the implantation damage and to activate the implanted dopant. By prolonging this laser annealing treatment, some diffusion of the implanted dopant at the edge of the undoped channel region 1 can be obtained.

Figure 6 shows experimental results of the improvement in hot-carrier degradation achieved using such an overlapped long field-relief region 5 in a TFT structure in accordance with the invention, as compared with a similar TFT structure without any field-relief region 5. The voltage value Vd 30% in Figure 6 is the value of drain voltage applied to the drain region 3 which produces a 30% drop in the on-current through the TFT within one minute of operation in the on-state. Therefore this voltage Vd 30% is a measure of hot carrier degradation of the on-current due to the electric field intensity between the channel region 1 and the drain region 3. Curve A in Figure 6 is for the TFT structure in accordance with the present invention, having the gate-overlapped long field-relief region 5. Curve B is for a similar TFT structure which does not have any field-relief region 5. In these TFT structures, the length L1 of channel region 1 was 6μm, the thickness of the silicon dioxide film 13 was 0.15μm, and the region 5 was provided in accordance with the invention with a phosphorous ion dose of 5.10^{17} cm^{-2} and a length L2 of 2μm overlapped by the gate

electrode 12. Both TFTs are in the off-state at Vg of 0 volts and only just on at Vg of 7.5 volts and are fully on at higher values of Vg. As can be seen from Figure 6, the inclusion of a gate-overlapped long field-relief region 5 in accordance with the present invention results in a very large increase in hot-carrier stability of the TFT, in both off and on states, and this improvement is achieved without an increase in series resistance.

Figures 1 and 2 illustrate the inclusion of a gate-overlapped field-relief region 5 in accordance with the present invention in a self-aligned implanted TFT structure. However, the present invention may be adopted in a wide variety of TFT structures. In the embodiment of Figures 1 and 2, the silicon film pattern 11 is formed from a single film, and the source and drain regions 2 and 3 and the field-relief region 5 are formed by locally doping areas of this single film. Figures 7 and 8 illustrate a TFT embodiment in accordance with the present invention in which the TFT silicon film pattern 11 comprises multiple films each having a different doping concentration.

In the TFT embodiment of Figures 7 and 8, the source and drain regions 2 and 3 are formed from a highly doped n+ silicon film deposited on the insulating substrate 10 and divided by etching to form the separate regions 2 and 3. The lower doped regions 4 and 5 are formed by depositing a lower doped silicon film 45 and then dividing it to separate the regions 4 and 5 which extend onto to the substrate 10 from over the regions 2 and 3. Finally, the channel region 1 is provided by depositing an undoped silicon film 45 over the thin film structure 3 and 5 and on the substrate 10. The resulting silicon thin-film structure 3, 5, 45 and 41 is then etched into the separate TFT islands 11 on the substrate 10. The low-doped regions 4 and 5 are formed by the parts of the film 45 which do not overlap the source and drain regions 2 and 3. The channel region 1 is formed by the area of the film 41 which does not overlap the film parts 45.

After depositing a gate dielectric film 13 of, for example, silicon dioxide, the gate electrode 12 is formed by providing a conductive film portion on the dielectric film 13 over the channel region 1 and over the low-doped regions 4 and 5. The resulting TFT structure is shown in Figure 7. There is a sharp

transition in the doping concentrations between the undoped layer 41, low-doped layer 45 and highly doped regions 2 and 3 because only low temperatures are used during the growth of the films 45 and 41 on the substrate 10. However, thermal diffusion and hence a noticeable grading of these doping concentrations can be achieved by a laser heating treatment of the thin-film structure of Figure 8. Thus, Figure 8 illustrates heating this film structure with an energy beam 50 from, for example, an excimer laser in order to diffuse the doping concentrations at the interfaces of the different films. This laser treatment may also be used to crystallise the film structure 2,3,45,41 into large-grain polycrystalline material.

Instead of or in addition to thermal diffusion, other process steps may be used to grade the doping concentration at the interfaces of the field-relief region 5 with the undoped channel region 1 and the highly doped drain region 3. Thus, for example, when ion implantation is used to provide the doping concentration, an edge of the implantation mask may be bevelled so as to grade the doping concentration implanted at this area. By way of example, Figure 2 shows a bevelled edge for the implantation mask 32 for the n- implant, and Figure 1 shows a bevelled edge for the gate implantation mask 13 for the n+ source and drain implant. In this embodiment of Figures 1 and 2, the doping concentration of the regions 4 and 5 is substantially uniform along the length L3 and L2 of these regions 4 and 5 except where graded at the interfaces with the undoped channel region 1 and the highly-doped source and drain regions 2 and 3.

Figure 9 shows a further modification in accordance with the present invention, in which the doped regions 2, 3, 4 and 5 are formed by a single implantation step into an undoped silicon single film 11. The implantation mask comprises the gate electrode 12 which has very long bevelled edges 34 and 35. These bevelled edges 34 and 35 are sufficiently long that the dopant ions implanted therethrough form the long low-doped regions 4 and 5 of length L3 and L2 between the undoped channel region 1 and the highly doped source and drain regions 2 and 3.

In the embodiments of Figures 1, 2 and 9 the gate electrode 12 is

formed as a single layer extending over the regions 1, 4 and 5. However, the gate electrode 12 may be formed by two overlapping layers, namely a first (narrow) layer over the channel region 1 and a second (wider) layer which extends also over the regions 4 and 5. The first narrow layer may provide an implantation mask 32 for masking the channel region 1 against an n- implant for the regions 4 and 5. The second wider layer may provide an implantation mask for the implantation step used to provide the n+ source and drain regions 2 and 3. Both the first and second layers may have bevelled edges to provide a graded doping concentration by implantation therethrough.

Figure 10 illustrates yet another TFT structure in accordance with the present invention. It comprises multiple films forming the semiconductor film pattern 11 of the TFT and may be considered to be a modification of the TFT structure of Figure 7. However, in the TFT of Figure 10, the undoped polycrystalline silicon film 41 which provides the channel region 1 is deposited on the insulating substrate 10 before depositing one or more doped polycrystalline films 46 for the regions 2 to 5. The doped regions 2 to 5 are formed by depositing the film or films 46 and then etching away areas of these films in order to define the lateral extent of the regions 1 to 5 and the TFT island 11. Thus, in this case, the drain region 3 and field-relief region 5 may be formed by a) depositing a semiconductor film 46 while increasing gradually the dopant content in the deposition gases so that the film 46 is deposited with a doping concentration which increases progressively from the field-relief region 5 (n-) to the drain region 3 (n+) and b) defining a interface between the drain region 3 and the adjacent part of the field-relief region 5 by etching away an area of the increased doping concentration to leave a bevelled surface 37 between the drain region 3 and the field-relief region 5. This etch definition in the specific example of Figure 10 also extends deeper to expose the channel region 1 and also forms a similar bevelled surface 37 at the source end of channel region 1. After providing the gate dielectric film 13, the overlapping gate electrode 12 is then provided on the dielectric film 13 over the channel region 1 and over the low-doped regions 4 and 5. The resulting structure is shown in Figure 10.

In the embodiments of Figures 1 to 10 the gate electrode 12 is formed at the upper face of the TFT structure remote from substrate 10. However, a TFT in accordance with the present invention may have a gate electrode 12 provided on the substrate 10 before depositing a gate dielectric film 13, after which a silicon film for the TFT body structure 11 is deposited. The TFT region structure 1 to 5 is formed subsequently in this semiconductor film by localised doping. Figure 11 illustrates such a modification at an ion implantation stage comparable to that of Figure 2. In this implantation stage the low doping concentration for the regions 4 and 5 is provided, while using an implantation mask 32 over the area which is to form the undoped channel region 1. The implantation mask 32 is present, in this example, on an insulating layer 39 on the silicon film 11. As can be seen from Figure 11 the gate electrode 12 is much wider than the undoped channel region 1, so that the subsequently formed field-relief region 5 overlaps this gate electrode 12.

When the silicon film or the TFT body 11 is crystallised by laser annealing, the laser anneal may be carried out after providing the doping concentrations for the regions 4 and 5 and/or the regions 2 and 3. In this case, the laser anneal may be used to thermally diffuse these doping concentrations so that a doping gradient is formed at the transitions between the regions 1 to 5. Such a laser annealing and diffusion treatment may be carried out after the implantation steps of Figures 2 and 11, and so it may also be used to anneal the implants.

The manufacture of N-channel TFTs having n-type regions 2 to 5 has been illustrated with reference to the drawings. However, the invention may also be used in the manufacture of p-channel devices, having highly-doped p-type source and drain regions 2 and 3 with a lower-doped p-type field-relief region 5 and (if desired) a similar low-doped region 4. In the embodiments described, the semiconductor film pattern 11 is of polycrystalline silicon. However TFTs may be manufactured in accordance with the present invention in and on semiconductor film patterns of amorphous silicon or of another disordered semiconductor material, for example cadmium selenide or cadmium sulphide.

From reading the present disclosure, other variations and modifications will be apparent to persons skilled in the art. Such variations and modifications may involve equivalents and other features which are already known in the design, manufacture and use of electronic devices comprising TFTs and other semiconductor devices and component parts thereof and which may be used instead of or in addition to features already described herein. Although Claims have been formulated in this Application to particular combinations of features, it should be understood that the scope of the disclosure of the present invention also includes any novel feature or any novel combination of features disclosed herein (either explicitly or implicitly) or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any Claim and whether or not it mitigates any or all of the same technical problems as does the present invention. The Applicants hereby give notice that new Claims may be formulated to such features and/or combinations of such features during the prosecution of the present Application or of any further Application derived therefrom.

CLAIMS

1. An electronic device including thin-film circuit elements which comprise a semiconductor film pattern on an insulating substrate, one of the circuit elements being a thin-film field-effect transistor having a gate electrode which overlaps and is coupled to an undoped channel region of the semiconductor film pattern for controlling current flow through the channel region, wherein the transistor has a field-relief region of one conductivity type between the undoped channel region and a drain region of the one conductivity type, the conductivity type determining doping concentration of the field-relief region being lower than that of the drain region, wherein the gate electrode overlaps and is coupled to the field-relief region, the overlapped length of the field-relief region being larger than the thickness of the semiconductor film pattern.

2. An electronic device as claimed in Claim 1, characterised in that the electric field along the overlapped length of the field-relief region exhibits a first peak between the channel region and the field-relief region and a second peak between the field-relief region and the drain region, and the doping concentration between the field-relief region and the drain region is graded to reduce the intensity of the second peak.

3. An electronic device as claimed in Claim 1 or Claim 2, characterised in that the electric field along the overlapped length of the field-relief region exhibits a first peak between the channel region and the field-relief region and a second peak between the field-relief region and the drain region, and the doping concentration of the field-relief region is graded into the channel region to reduce the intensity of the first peak.

4. An electronic device as claimed in any one of the preceding Claims, characterised in that the doping concentration from the field-relief region to the drain region and/or channel region is graded so as to vary

progressively over at least 20%, preferably a third or more, of the entire length of the field-relief region between the channel region and the drain region.

5. An electronic device as claimed in any one of the preceding Claims, further characterised in that the overlapped length of the field-relief region is in excess of 1 μm (micrometre), and preferably is sufficiently long to separate a first peak occurring in the electric field between the channel region and the field-relief region from a second peak occurring in the electric field between the field-relief region and the drain region.

6. An electronic device as claimed in any one of the preceding Claims, further characterised in that the conductivity type determining doping concentration of the field-relief region is of the order of 10^{17} cm^{-3}, for example about 5×10^{17} cm^{-3}.

7. A method of manufacturing an electronic device as claimed in any one of Claims 1 to 6, wherein the doping concentration of the drain region is provided by dopant ion implantation while using the gate electrode as a mask, the edge of the gate electrode being bevelled so as to grade the implanted doping concentration from the drain region to the field-relief region.

8. A method of manufacturing an electronic device as claimed in any one of Claims 1 to 6, wherein the drain region and at least the adjacent part of the field-relief region are formed by (a) depositing a semiconductor film with a doping concentration which increases progressively from the field-relief region to the drain region, and (b) defining an interface between the drain region and the adjacent part of the field-relief region by etching away an area of the increased doping concentration to leave, for example, a bevelled surface between the drain region and the field-relief region.

9. A method of manufacturing an electronic device as claimed in any one of Claims 1 to 6, wherein the doping concentration of the drain region is

diffused into the field-relief region to grade the doping concentration between the field-relief region and the drain region.

10. An electronic device having any one of the novel features described herein and/or illustrated in the accompanying drawings, or manufactured by a method having any one of the novel features described herein and/or illustrated in the accompanying drawings.

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Application No: GB 9711325.2
Claims searched: 1-9

Examiner: SJ Morgan
Date of search: 19 June 1998

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): H1K(CAA)

Int Cl (Ed.6): H01L 21/336, 29/786

Other: Online:WPI,JAPIO,CLAIMS,INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	US 5 612 234 (LG ELECTRONICS) Note regions 42a, 42e in figure 6F.	
X	Proceedings of the 1996 International Active Matrix Workshop, pp 33-36 1996, "Influence of drain field on poly-Si TFT behaviour" JR Ayres & SD Brotherton.	1-3 & 5
X	Japanese Journal of Applied Physics, Vol 36, pp 1522-1524, Part 1, No 3b, March 1997, "A novel LDD structured poly-Si thin film transistor with high on/off ratio" Kwon-Young Choi et. al.	1
X	IEEE Electron Device Letters, Vol 17, No 12, December 1996, "A novel gate-overlapped LDD poly-Si thin film transistor", Kwon-Young Choi & Min-Koo Han.	1

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